عنوان مقاله:

FPGA Implementation of JPEG and JPEG۲۰۰۰-Based Dynamic Partial Reconfiguration on SOC for Remote Sensing Satellite On-Board Processing

محل انتشار:

فصلنامه علوم و فناوری فضایی, دوره 7, شماره 1 (سال: 1393)

تعداد صفحات اصل مقاله: 10

نویسندگان:

A. Chekini

H. R. Naji

خلاصه مقاله:

This paper presents the design procedure and implementation results of a proposed hardware which performs different satellite Image compressions using FPGA Xilinx board. First, the method is described and then VHDL code is written and synthesized by ISE software of Xilinx Company. The results show that it is easy and useful to design, develop and implement the hardware image compressor using new techniques of programmable logic tools for space applications. In this paper the proposed hardware uses the proposed hardware, and it is put on board of satellite. Appropriate bit streams are produced by synthesis tools; therefore, we have two bit streams which can be configured at any moment of time according to the user request. When users intend the hardware is reconfigured and changed from JPEG to JPEG۲۰۰۰ or vice versa. The Proposed architecture has some advantages other than previous architectures such as high-speed and real-time processing, high flexibility, low cost, high security and low power consumption. This idea can be utilized in modern commercial hardware space board for data compressing due to using partial reconfiguration technique.

کلمات کلیدی:

compression, satellite, on, Board Processing, real, Time Processing, Reconfigurable