عنوان مقاله:

A New Low Power-Delay-Product, Low-area, Parallel Prefix Adder With Reduction of Graph Energy

محل انتشار:

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نویسندگان:

M. Moghaddam - *Dept. of Electrical Engineering Shahed University Tehran – IRAN*

M. B. Ghaznavi-Ghoushchi

خلاصه مقاله:

In this paper the graph energy and electrical power consumption of various parallel prefix adders (PPA) are measured and investigated. By comparison the graph energy of PPAs with their power consumption, a linear relation between them is considered. Moreover, the measurements represent direct relation between arcs number and graph energy in PPA structures. Using these results a new PPA (proposed I) is introduced that it is achieved from Sklansky adder with reduction of graph energy and limiting the recursive stages to maximum 8 steps. A new standard, product of arc numbers and logic depth, is applied to compare the performance of proposed adder I with other PPAs. In addition using even and odd cells in proposed adder I resulted in proposed adder II. All the simulations are done with Hspice and CMOS technology 180nm. Simulation results represent that power-delay-product of our 32-bit proposed adder I and II come with about 17% and 35% improvement compared with Sklansky adder, respectively.

کلمات کلیدی:

Parallel Prefix Adders, Sklansky Adder, Lowpower, Low-Area, CMOS Circuits, Graph Energy