عنوان مقاله:

A 4.2GHz, 3.3mW, 1.1pJ, 90nm 64-bit New Digital Comparator with 1.2 Clock Pipeline Delay

محل انتشار:

نوزدهمین کنفرانس مهندسی برق ایران (سال: 1390)

تعداد صفحات اصل مقاله: 6

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خلاصه مقاله:

This paper presents a new digital comparator. It is based on the general form of the n-bit digital comparators with majority functions. We propose a target system of 64-bit digital comparator built on the top of a modified and improved Domino Logic with pipeline structure. Our design comes without the inter-block inverters of the conventional domino logics. The proposed comparator is evaluated in 90nm at 1.2v VDD at clock frequency of 4.2GHz with 1.2 clock cycle delay or 310 picoseconds. The power and Power-Delay-Products in 90nmare 3.3mw and 1.12pJ respectively. To show the effectiveness of our proposed approach, we evaluate our design with 90nm PTM at the clock rate of 5.4GHz or about 50% improvement against the best known previous digital comparator. Furthermore, simulation of our design in AMI 0.5um at 5v VDD shows 2.0 GHz clock speed and 1.5 clock cycle delay or 750 picoseconds. This in turn has about 43% improvement against best known digital comparator at this technology

کلمات کلیدی:

High speed digital comparators, Domino Logic, Dynamic CMOS Logic