عنوان مقاله:

An Ultra-low Power Ternary Multi-digit Adder Applies GDI Method for Binary Operations

محل انتشار:

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خلاصه مقاله:

kground and Objectives: This paper introduces a novel low-power and low-delay multi-digit ternary adder in carbon nanotube field effect transistor (CNTFET) technology. Methods: In the proposed design, reducing the power consumption is the main priority. In this multi valued logic design, geometry-dependent threshold voltage of the CNTFET is the design code. At each stage, a half adder is applied to generate the intermediate binary signals called half-sum (HS) and half-carry (HC). For the binary operations, the gate diffusion input (GDI) method is used to significantly reduce the power consumption as in the proposed decoder design. Results: In this work a GDI based sum generator and a low-power encoder are used to calculate the final sum value of each stage. Furthermore, the proposed carry generation/propagation block results in a significant reduction in the overall propagation delay time. The simulation reveals a significant improvement in terms of power consumption (up to ۲۷%), PDP (up to ۴۱%) and FO۴ delay (up to ۲۰%).Conclusion: A CNTFET based power and delay efficient multi-digit ternary adder has been presented in this paper. The simulation is performed by the Synopsis HSPICE simulator with Stanford ۳۲ nm CNTFET technology. According to the results, a significant saving in average power consumption is achieved where the power-delay product (PDP) is improved by ۴۱% compared to the best existing design.

کلمات کلیدی:

CNTFET, Low power Adder, Ternary logic, Multi-valued logic, GDI