عنوان مقاله:

A New Net list Generator for Simulation of High Performance Nano-Scale Interconnects

محل انتشار:

دومین کنگره بین المللی علوم و فناوری نانو (سال: 1387)

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خلاصه مقاله:

The trend of IC technologies has been approaching nanometer scale. The all wire dies are now becoming a reality where nanoscale interconnects heavily impact the performance of high speed digital and analog integrated circuits [1, 2 and 4]. With scaling down of technology feature sizes to nano scale dimensions, the interconnect resistance and coupling capacitance plays an important role in determining the delay and coupling effects in VLSI circuits [3, 6]. Since invention of MOS transistor at Bell Telephone Laboratories in 1947, many CAD tools have been developed in electronics domain to provide the ability to simulate transistor based circuits. Some of these simulators run for the post layout simulation; while others can simulate in higher levels of abstraction. It is obvious that the simulation in transistor level is more accurate than that of in the gate level [5]. Hence, the necessity to have a tool that gives us the ability to simulate the circuits with taking into account the effects of nano scale interconnects as an input for a more accurate simulation in transistor level has been the principle motivation to build our home-made CAD tool. This tool generates a net list which is useful for transistor level circuit simulation which includes the equivalent circuit model of the nano scale interconnect

کلمات کلیدی: