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عنوان مقاله:

Design and Implementation of an N-type Integer Phase-locked Loop with Low Phase Noise and Two Output Frequencies at ۱ and ۴ GHz

محل انتشار:

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خلاصه مقاله:

This article presents development and implementation of an integer N-type Phase Locked Loop (PLL) module with two output frequencies of ۱ and ۴ GHz, each having a phase noise better than -۱۱۰dBC/Hz@۱۰k. The structure has ۰ and ۱۰dBm power levels at ۱ and ۴GHz output frequencies, respectively. Having two different outputs of ۱ and ۴ GHz at once, in addition to the ۱.۱ and ۴.۴GHz realized by the capability included in this design in which two additional outputs can be achieved by using the pins A۰ to A۴ and altering their status, makes this structure a good candidate for mass production. A two-step frequency division is employed in this work. The first step is realized using the frequency divider of order ۴, and the second step is implemented inside the HMC۴۴۰ IC, including a PFD and a counter. Compared to typical methods, this method presents a clean output by suppressing the spurs meant to be manifested using a single-step frequency division. This PLL is constructed in discrete and modular modes and employed in transceivers' up-converter and down-converter blocks, Satellite communications, Cable TV links (CATV), Local Area Networks (LAN), Global Positioning Systems (GPS), test equipment, digital radios, military and commercial communications. For a specific example, the ۴GHz frequency is used to up-converte or down-converte the received signals, and the ۱-GHz frequency is usually used for the synthesizer module clock frequency. Advanced Design System (ADS) was used in the design, and OrCAD was used in the schematic design of the PLL module.

کلمات کلیدی:

Phase Lock Loop, Phase Noise, Low Phase Noise, Spur

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