عنوان مقاله:
Novel Design of Array Multiplier

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خلاصه مقاله:
In this paper a new array multiplier has been proposed, which has lower power consumption than the regular array multipliers. This technique has been applied on two conventional and leapfrog array multipliers. In the formation of 8×8 multiplier all designs proposed in this paper have been implemented using the HSPICE by the use of 180 nm TSMC technology at a supply voltage 1v. To verify the performance of the proposed structures, structures have been simulated in 130 nm & 65 nm PTM technologies. The simulation results show that applying the return technique in the array structures causes power consumption reduction and consequently PDP reduction. This improvement for 180 nm technology in the conventional array structure is 13.32 % and in the leapfrog array structure is 23.27 %. It should be noted that this technique substantially makes the number of transistors less and as a result area reduction

کلمات کلیدی:
array multiplier, return technique, return leapfrog array multiplier, power, delay