

عنوان مقاله:

A 3 GHz CMOS DLL-Based Frequency Multiplier

محل انتشار:

شانزدهمین کنفرانس مهندسی برق ایران (سال: 1387)

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خلاصه مقاله:

In this paper, a DLL-based frequency multiplier is presented. By utilizing an inductor in power supply and ground rails, the maximum frequency of the multiplier's output reaches 3 GHz for a 750 MHz input. The inductor used in the multiplier is smaller than 10nH and can be implemented as spiral inductor. The multiplication factor is four for eight delayed voltage controlled delay line (VCDL) output clocks. Hspice simulation results using a 0.18 _m CMOS technology show that the multiplier power dissipation is as low as 5.5 mW. The cycle to cycle jitter is 32ps and the area of the circuit is 20547m

كلمات كليدي:

Delayed Locked Loop, Edge Combiner, Frequency Multiplier, Phase Frequency Detector, Voltage Controlled Delay

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