

## عنوان مقاله:

A Technique For Testing Network Connections In Parallel With Mesh Topology

## محل انتشار:

چهارمین کنفرانس بین المللی پژوهش های نوین در علوم مهندسی و تکنولوژی (سال: 1394)

تعداد صفحات اصل مقاله: 15

## نویسندگان:

javad mohajerani - Department of computer engineering, Baft branch, Islamic azad university, Baft, Iran

farokh kourpoi - Department of computer engineering, Baft branch, Islamic azad university, Baft Iran

## خلاصه مقاله:

In this paper, we connections between switches in the mesh network topology in a parallel way we've tested. The method is based on a built-in self-test, the use of buffers FIFO Each of the switches, test all connections between switches is done in parallel, not only test application time, but the area overhead of the network is reduced. The demands of future computing and high-density integrated circuit design challenges for nanometer technology requires new methods and styles in the design, which is certainly the method of high performance and low power consumption as well as high resistance to noise and changes The process will have. One of the main problems, mechanism of communication that must increase the number of blocks or cells that can be embedded in a chip, is established. The bus-based systems and point-to-point communication strategy can not easily embedded cores inside a single chip together a large number of systems-on-chip designers, and so great is faced with many restrictions. Network-on-chip communication infrastructure, one of the key technologies that many design constraints-on-chip systems for large multi-core processors to eliminate the source of the emergence of system-on-chip with high computing power low power consumption. This treatise on network-on-chip testing of the communication infrastructure is concentrated. Motivation to do it is with the continuing miniaturization of circuits in nanometer technology, flaws and bugs a serious challenge for manufacturing integrated circuits with millions of transistors will be. So solutions need to be network-on-chip communication infrastructure bug detector is developed. In this study, a built-in self-test procedure to test the link between high-performance switches have been suggested to play a role in significantly reducing application time-tested play. In this way, using the built-in self-test, simultaneous testing of all network-on-chip communication infrastructure links in a testing session provides a fully parallel so that all communication links are tested when user testing can be minimized

## کلمات کلیدی:

Built-In Self-Test, Hearing , Connections, Network With Mesh Topology

## لینک ثابت مقاله در پایگاه سیویلیکا:

<https://civilica.com/doc/482267>



