عنوان مقاله:

Wide-Range, Low-Jitter Frequency Synthesizer Using Common Mode DC Setting Strategy in VCDL

محل انتشار:

اولین کنفرانس بین المللی دستاوردهای نوین پژوهشی در مهندسی برق و کامپیوتر (سال: 1395)

تعداد صفحات اصل مقاله: 5

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خلاصه مقاله:

A low jitter, multi-phase delay-locked loop based frequency synthesizer for wide locking range with simple and openloop phase detector is proposed. Dead-Zone of the proposed PD is improved in compare to the conventional structures where the pulse generator postpones PD response and reduces the sensitivity. Also, the conventional structure of delay cells is modified, given a supplied reference input with 50% duty cycle, the DLL generates an output clock with the duty cycle of nearly 50% over the entire operating frequency range. Moreover the results show that the dead-zone of the phase detector and jitter of the outputs are reduced as well. Worst-Case simulation results in post-layout simulations for all corners, using the BSIM3 model of 0.18um CMOS process when the supply voltage is subject to around 30mvolts peak-to-peak noise disturbances confirm that DLL loop can provide phases in frequency range of 20MHZ to 200MHz, consuming total power of 6.8mW at 200MHz. The designed chip occupies an area of .0.06 mm2

کلمات کلیدی:

Delay Locked Loop, Frequency Synthesizer, Low Jitter DLL, Dead-Zone, Phase Detector