عنوان مقاله:

Design of High-Speed Low-Power Dynamic Latched Comparator for Pipeline ADC Applications

محل انتشار:

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خلاصه مقاله:

Analogue comparator along with preamplifier requires higher amount of current rather than the latch circuitry. This paper presents the design and analysis of a latch basedvoltage comparator using charge sharing circuit topology for low-power and high-speed applications such as pipeline ADCs.The focus of this design is minimization of propagation delay and power consumption of the comparator, which will improve the comparator performance. Compared to state-of-the-art powerefficientlatched comparators, this comparator provides lower power dissipation due to careful layout design and optimization.Simulation results have been obtained using 90nm TSMC-CMOS technology, for a 200MHz clocked comparator, considering 1 Vsupply voltage and 1V input range. Schematic and post-layout simulations along with Monte-Carlo analysis to define inputreferreddynamic offset voltage are verified using Cadence- Virtuoso designing tools

کلمات کلیدی:

analog to digital comparator (ADC); charge sharing comparator; low-power; propagation delay