## عنوان مقاله:

(DOUBLE EDGE TRIGGERED MODIFIED HYBRID LATCH FLIPFLOP (DMHLFF

## محل انتشار:

دوازدهیمن کنفرانس مهندسی برق ایران (سال: 1383)

تعداد صفحات اصل مقاله: 6

## نویسندگان:

S. H. Rasouli - *IC Design Laboratory, Electrical and Computer Engineering Dept., University of Tehran, Tehran*

A Afzali-Kusha - *IC Design Laboratory, Electrical and Computer Engineering Dept., University of Tehran*

*(*A Khadem-zadeh - *Iran Telecom. Research Center (ITRC*

M Nourani - *Department of Electrical Engineering, University of Texas at Dallas*

## خلاصه مقاله:

In this paper a new low power flip-flop called Double-edge triggered Modified Hybrid Latch Flip-Flop (DMHLFF) has been proposed and compared to previous flip-flops. DMHLFF is a low power, low area, and fast flip-flop. Power consumption is reduced by avoiding unnecessary internal node transition. Power consumption in clock tree is also reduced by decreasing the frequency of clock to half f the cock frequency in single edge triggered flipflop for the same throughput. These capabilities are obtained by modifying the structure of conventional Hybrid Latch Flip-Flop without any penalty in area. Reducing the number of transistor in stack leads to having less delay and thus higher operational speed compared to others flip-flops

## کلمات کلیدی:

low power, Edge-triggered flip-flop, node transition, LFSR