

عنوان مقاله:

A Novel Technique for Reducing Subthreshold Current of VLSI Combinational Circuits

محل انتشار:

دوازدهیمن کنفرانس مهندسی برق ایران (سال: 1383)

تعداد صفحات اصل مقاله: 5

نویسندگان: J. Jafari - *IC Design Lab., ECE Dept., University of Tehran*

A Amirabadi - IC Design Lab., ECE Dept., University of Tehran

A. Afzali-Kusha - IC Design Lab., ECE Dept., University of Tehran

خلاصه مقاله:

In this paper, a new technique for reducing the subthreshold leakage current of CMOS VLSI circuits is proposed. It makes use of the fact that leakage currents of gates are depended on their input patterns. The order of gate input lines is manipulated to reduce the leakage current. The key feature of the method is that it does not have any overhead on the area or the speed. Also, it does not affect the dynamic power consumption of the gate. The execution time for the algorithm determining the primary input order is also very fast. Up to 12% of the static power reduction is .achieved by applying this method to ISCAS85 benchmark circuits

کلمات کلیدی: VLSI, Low power Combinational Circuits, Standby power, Subthreshold Leakage Current

لینک ثابت مقاله در پایگاه سیویلیکا:

https://civilica.com/doc/59850

