عنوان مقاله:

Low-Power Level-Shifting Architecture for Sub-threshold Logic Circuits

محل انتشار:

مجله سیستم های برق و سیگنال, دوره 2, شماره 2 (سال: 1393)

تعداد صفحات اصل مقاله: 6

نویسندگان:

.Seyed Rasool Hosseini - *Departmant of Electrical Engineering, Ferdowsi University of Mashhad, Iran*

.Mehdi Saberi - *Departmant of Electrical Engineering, Ferdowsi University of Mashhad, Iran*

.Reza Lotfi - *Departmant of Electrical Engineering, Ferdowsi University of Mashhad, Iran*

خلاصه مقاله:

This paper presents a power-efficient voltage level shifter converting low levels of input voltages (sub-threshold) to high levels of the output voltages (above threshold). In order to reduce the existing contention in the output nodes between pull-up and pull-down devices, the proposed circuit uses a current generator to reduce the strength of the pull-up device when the pull-down device is pulling down the output node. This causes the circuit to be functional even for the sub-threshold input voltages. In order to avoid the static power dissipation, this current generator turns on only during the transition times in which the logic level of the input signal is not corresponding to the output logic level. Simulation results of the proposed circuit in a 0.18-µm technology confirm that for a low supply voltage of VDDL = 0.42 V at the input and a high supply voltage of VDDH = 1.8 V at the output, the level shifter has a propagation delay .of 22 ns, an energy per transition of 340 fJ, and a static power dissipation of 0.42 nW for 1-M Hz input signal

کلمات کلیدی:

Level shifter, level converter, sub-threshold, low power operation, dual supply