عنوان مقاله:
A Dynamic Double-edge-triggered D-type Flip-Flop

محل انتشار:
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خلاصه مقاله:
A dynamic negative-edge-triggered D-type flip-flop (D-NETFF) with four clocked transistors is developed based on the true single-phase clock (TSPC) dynamic technique. The performance of the D-NETFF is compared with that of a static master-slave D-type flip-flop in a 90nm CMOS technology based on SPICE simulations. Furthermore, the DNETFF is combined with its positive edge-triggered equivalent, D-PETFF in a single topology using a 2:1 multiplexer to develop a dynamic double-edge-triggered D-type flip-flop (DETFF). Operating with a 0.9-V power supply at a clock frequency of 16.7 GHz, the proposed DETFF exhibits an average Clock-to-Q delay of 25 psec and consumes 486 µW in a 20nm CMOS technology. Compared with common static latch-based flip-flops, dynamic TSPC flip-flops are faster, employ a smaller number of transistors and consume less power.

کلمات کلیدی:
D flip-flop, double-edge clocking, dynamic circuits, true single-phase clock